

# MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® Hex Buffers MM70C96/MM80C96, MM70C98/MM80C98 TRI-STATE Hex Inverters

## General Description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The MM70C95/MM80C95 and the MM70C97/MM80C97 convert CMOS or TTL outputs to TRI-STATE outputs with no logic inversion, the MM70C96/MM80C96 and the MM70C98/MM80C98 provide the logical opposite of the input signal. The MM70C95/MM80C95 and the MM70C96/MM80C96 have common TRI-STATE controls for all six devices. The MM70C97/MM80C97 and the MM70C98/MM80C98 have two TRI-STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to  $V_{CC}$  and GND.

## Features

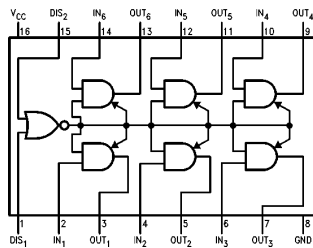
- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity  $0.45 V_{CC}$  (typ.)
- TTL compatible Drive 1 TTL Load

## Applications

- Bus drivers Typical propagation delay into 150 pF load is 40 ns

## Connection Diagrams (Dual-In-Line Packages)

**MM70C95/MM80C95**

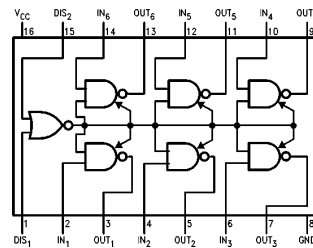


TL/F/5907-1

**Top View**

Order Number MM70C95 or MM80C95

**MM70C96/MM80C96**

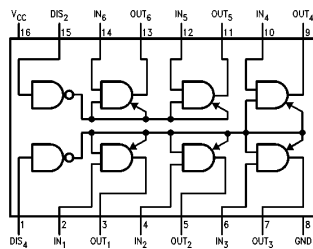


TL/F/5907-2

**Top View**

Order Number MM70C96 or MM80C96

**MM70C97/MM80C97**

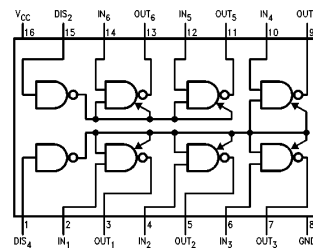


TL/F/5907-3

**Top View**

Order Number MM70C97 or MM80C97

**MM70C98/MM80C98**



TL/F/5907-4

**Top View**

Order Number MM70C98 or MM80C98

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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                             |                          |
|-----------------------------|--------------------------|
| Voltage at Any Pin          | −0.3V to $V_{CC} + 0.3V$ |
| Operating Temperature Range | −55°C to +125°C          |
| MM70CXX                     | −40°C to +85°C           |
| MM80CXX                     |                          |

|                                   |                 |
|-----------------------------------|-----------------|
| Storage Temperature Range         | −65°C to +150°C |
| Power Dissipation ( $P_D$ )       |                 |
| Dual-In-Line                      | 700 mW          |
| Small Outline                     | 500 mW          |
| Power Supply Voltage ( $V_{CC}$ ) | 18V             |
| Lead Temperature                  |                 |
| (Soldering, 10 seconds)           | 260°C           |

## DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

| Symbol              | Parameter                              | Conditions                                            | Min        | Typ             | Max        | Units              |
|---------------------|----------------------------------------|-------------------------------------------------------|------------|-----------------|------------|--------------------|
| <b>CMOS TO CMOS</b> |                                        |                                                       |            |                 |            |                    |
| $V_{IN(1)}$         | Logical “1” Input Voltage              | $V_{CC} = 5V$<br>$V_{CC} = 10V$                       | 3.5<br>8.0 |                 |            | V<br>V             |
| $V_{IN(0)}$         | Logical “0” Input Voltage              | $V_{CC} = 5V$<br>$V_{CC} = 10V$                       |            |                 | 1.5<br>2.0 | V<br>V             |
| $V_{OUT(1)}$        | Logical “1” Output Voltage             | $V_{CC} = 5V$<br>$V_{CC} = 10V$                       | 4.5<br>9.0 |                 |            | V<br>V             |
| $V_{OUT(0)}$        | Logical “0” Output Voltage             | $V_{CC} = 5V$<br>$V_{CC} = 10V$                       |            |                 | 0.5<br>1.0 | V<br>V             |
| $I_{IN(1)}$         | Logical “1” Input Current              | $V_{CC} = 15V$                                        |            | 0.005           | 1.0        | $\mu A$            |
| $I_{IN(0)}$         | Logical “0” Input Current              |                                                       | −1.0       | −0.005          |            | $\mu A$            |
| $I_{OZ}$            | Output Current in High Impedance State | $V_{CC} = 15V, V_O = 15V$<br>$V_{CC} = 15V, V_O = 0V$ | −1.0       | 0.005<br>−0.005 | 1.0        | $\mu A$<br>$\mu A$ |
| $I_{CC}$            | Supply Current                         | $V_{CC} = 15V$                                        |            | 0.01            | 15         | $\mu A$            |

## TTL INTERFACE

|              |                            |                                                                           |                                  |  |            |        |
|--------------|----------------------------|---------------------------------------------------------------------------|----------------------------------|--|------------|--------|
| $V_{IN(1)}$  | Logical “1” Input Voltage  | 70C $V_{CC} = 4.5V$<br>80C $V_{CC} = 4.75V$                               | $V_{CC} - 1.5$<br>$V_{CC} - 1.5$ |  |            | V<br>V |
| $V_{IN(0)}$  | Logical “0” Input Voltage  | 70C $V_{CC} = 4.5V$<br>80C $V_{CC} = 4.75V$                               |                                  |  | 0.8<br>0.8 | V<br>V |
| $V_{OUT(1)}$ | Logical “1” Output Voltage | 70C $V_{CC} = 4.5V, I_O = -1.6 mA$<br>80C $V_{CC} = 4.75V, I_O = -1.6 mA$ | 2.4<br>2.4                       |  |            | V<br>V |
| $V_{OUT(0)}$ | Logical “0” Output Voltage | 70C $V_{CC} = 4.5V, I_O = 1.6 mA$<br>80C $V_{CC} = 4.75V, I_O = 1.6 mA$   |                                  |  | 0.4<br>0.4 | V<br>V |

## OUTPUT DRIVE (Short Circuit Current)

|              |                       |                                                                        |       |  |  |    |
|--------------|-----------------------|------------------------------------------------------------------------|-------|--|--|----|
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 5V, V_{IN(1)} = 5V$<br>$T_A = 25^\circ C, V_{OUT} = 0V$      | −4.35 |  |  | mA |
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 10V, V_{IN(1)} = 10V$<br>$T_A = 25^\circ C, V_{OUT} = 0V$    | −20   |  |  | mA |
| $I_{SINK}$   | Output Sink Current   | $V_{CC} = 5V, V_{IN(0)} = 0V$<br>$T_A = 25^\circ C, V_{OUT} = V_{CC}$  | 4.35  |  |  | mA |
| $I_{SINK}$   | Output Sink Current   | $V_{CC} = 10V, V_{IN(0)} = 0V$<br>$T_A = 25^\circ C, V_{OUT} = V_{CC}$ | 20    |  |  | mA |

**Note 1:** “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the device should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

## AC Electrical Characteristics\* $T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , unless otherwise noted.

| Symbol                | Parameter                                                                                                                                                       | Conditions                                                                                                                                                                                                                                    | Min | Typ                                             | Max                                                | Units                                        |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------------------------------------|----------------------------------------------------|----------------------------------------------|
| $t_{pd0}$ , $t_{pd1}$ | Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output<br>MM70C95/MM80C95, MM70C97/MM80C97<br>MM70C96/MM80C96, MM70C98/MM80C98        | $V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$<br>$V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$                                                                                                                                                |     | 60<br>25<br>70<br>35                            | 100<br>40<br>150<br>75                             | ns<br>ns<br>ns<br>ns                         |
| $t_{pd0}$ , $t_{pd1}$ | Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output<br>MM70C95/MM80C95, MM70C97/MM80C97<br>MM70C96/MM80C96, MM70C98/MM80C98        | $V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$<br>$V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$<br>$V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$<br>$V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$                                                |     | 85<br>40<br>95<br>45                            | 160<br>80<br>210<br>110                            | ns<br>ns<br>ns<br>ns                         |
| $t_{1H}$ , $t_{0H}$   | Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0")<br>MM70C95/MM80C95<br>MM70C96/MM80C96<br>MM70C97/MM80C97<br>MM70C98/MM80C98 | $R_L = 10\text{k}$ , $C_L = 5\text{ pF}$<br>$V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$<br>$V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$<br>$V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$<br>$V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$  |     | 80<br>50<br>100<br>70<br>70<br>50<br>90<br>70   | 135<br>90<br>180<br>125<br>125<br>90<br>170<br>125 | ns<br>ns<br>ns<br>ns<br>ns<br>ns<br>ns<br>ns |
| $t_{H1}$ , $t_{H0}$   | Delay from Disable Input to Logical "1" Level (from High Impedance State)<br>MM70C95/MM80C95<br>MM70C96/MM80C96<br>MM70C97/MM80C97<br>MM70C98/MM80C98           | $R_L = 10\text{k}$ , $C_L = 50\text{ pF}$<br>$V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$<br>$V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$<br>$V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$<br>$V_{CC} = 5\text{V}$<br>$V_{CC} = 10\text{V}$ |     | 120<br>50<br>130<br>60<br>95<br>40<br>120<br>50 | 200<br>90<br>225<br>110<br>175<br>80<br>200<br>90  | ns<br>ns<br>ns<br>ns<br>ns<br>ns<br>ns<br>ns |
| $C_{IN}$              | Input Capacitance                                                                                                                                               | Any Input (Note 2)                                                                                                                                                                                                                            |     | 5.0                                             |                                                    | pF                                           |
| $C_{OUT}$             | Output Capacitance TRI-STATE                                                                                                                                    | Any Output (Note 2)                                                                                                                                                                                                                           |     | 11                                              |                                                    | pF                                           |
| $C_{PD}$              | Power Dissipation Capacitance                                                                                                                                   | (Note 3)                                                                                                                                                                                                                                      |     | 60                                              |                                                    | pF                                           |

\*AC Parameters are guaranteed by DC correlated testing.

## Truth Tables

MM70C95/MM80C95

| Disable<br>DIS <sub>1</sub> | Input<br>DIS <sub>2</sub> | Input | Output |
|-----------------------------|---------------------------|-------|--------|
| 0                           | 0                         | 0     | 0      |
| 0                           | 0                         | 1     | 1      |
| 0                           | 1                         | X     | H-z    |
| 1                           | 0                         | X     | H-z    |
| 1                           | 1                         | X     | H-z    |

MM70C96/MM80C96

| Disable<br>DIS <sub>1</sub> | Input<br>DIS <sub>2</sub> | Input | Output |
|-----------------------------|---------------------------|-------|--------|
| 0                           | 0                         | 0     | 1      |
| 0                           | 0                         | 1     | 0      |
| 0                           | 1                         | X     | H-z    |
| 1                           | 0                         | X     | H-z    |
| 1                           | 1                         | X     | H-z    |

MM70C97/MM80C97

| Disable<br>DIS <sub>4</sub> | Input<br>DIS <sub>2</sub> | Input | Output |
|-----------------------------|---------------------------|-------|--------|
| 0                           | 0                         | 0     | 0      |
| 0                           | 0                         | 1     | 1      |
| X                           | 1                         | X     | H-z*   |
| 1                           | X                         | X     | H-z**  |

MM70C98/MM80C98

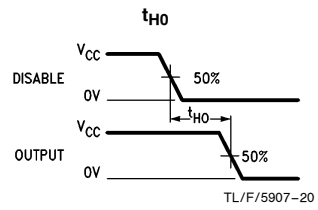
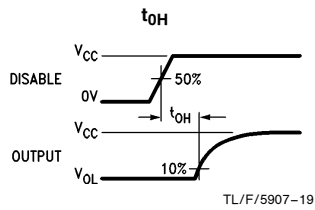
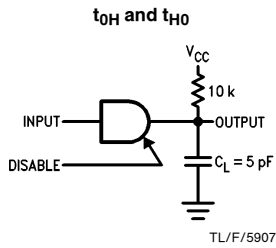
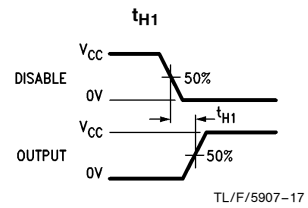
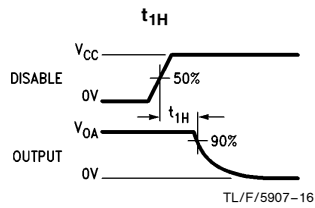
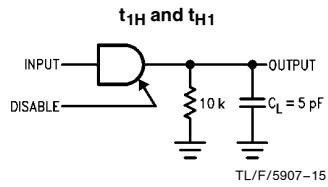
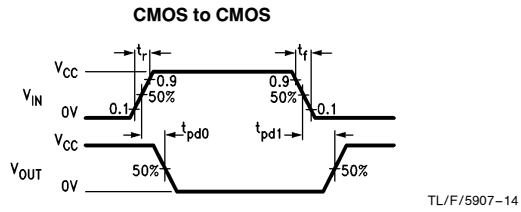
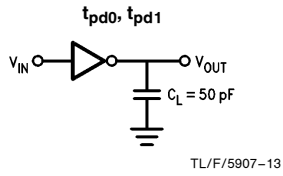
| Disable<br>DIS <sub>4</sub> | Input<br>DIS <sub>2</sub> | Input | Output |
|-----------------------------|---------------------------|-------|--------|
| 0                           | 0                         | 0     | 1      |
| 0                           | 0                         | 1     | 0      |
| X                           | 1                         | X     | H-z*   |
| 1                           | X                         | X     | H-z**  |

\*Output 5–6 only

\*\*Output 1–4 only

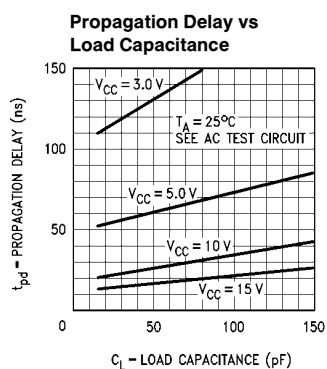
X = Irrelevant

## AC Test Circuits and Switching Time Waveforms

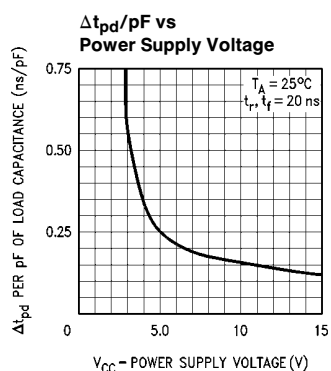


**Note:** Delays measured with input  $t_r$ ,  $t_f \leq 20$  ns.

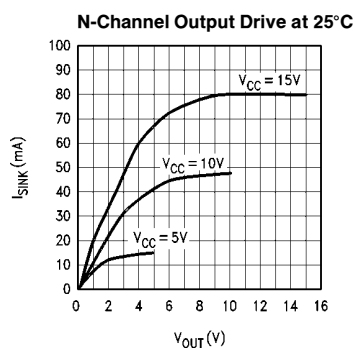
## Typical Performance Characteristics



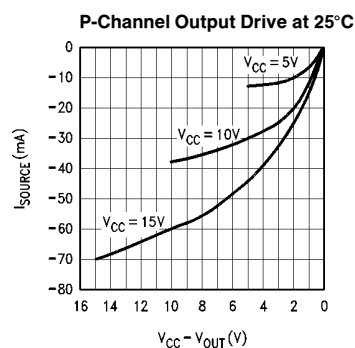
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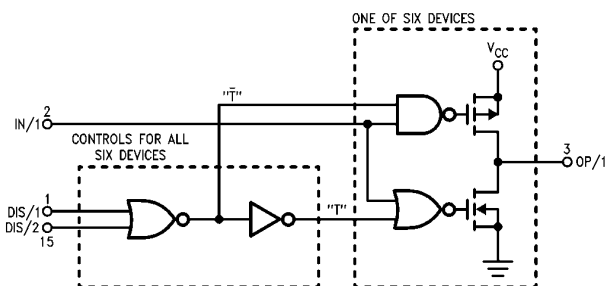
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TL/F/5907-8

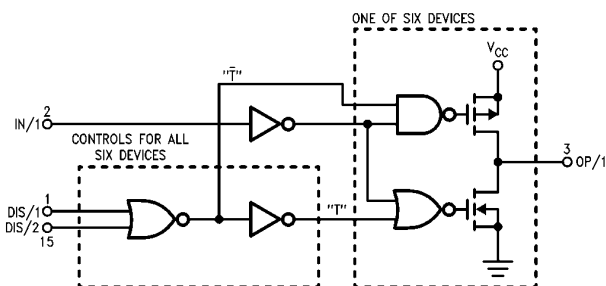
## Schematic Diagrams

## MM70C95/MM80C95 TRI-STATE



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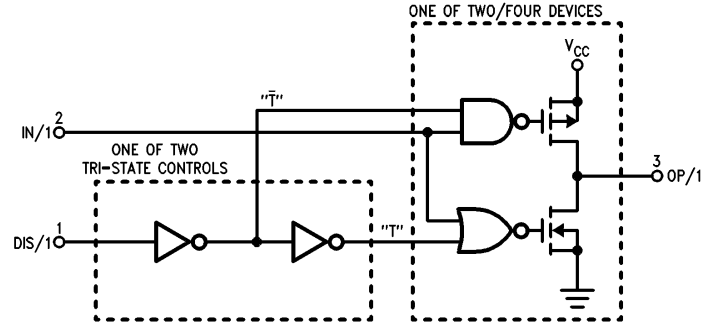
## MM70C96/MM80C96 TRI-STATE



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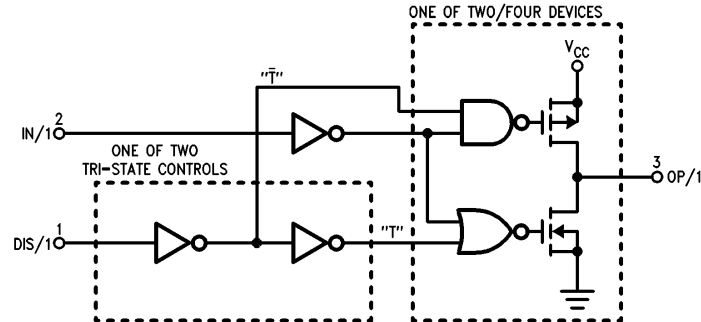
**Schematic Diagrams** (Continued)

**MM70C97/MM80C97 TRI-STATE**



TL/F/5907-11

**MM70C98/MM80C98 TRI-STATE**



TL/F/5907-12

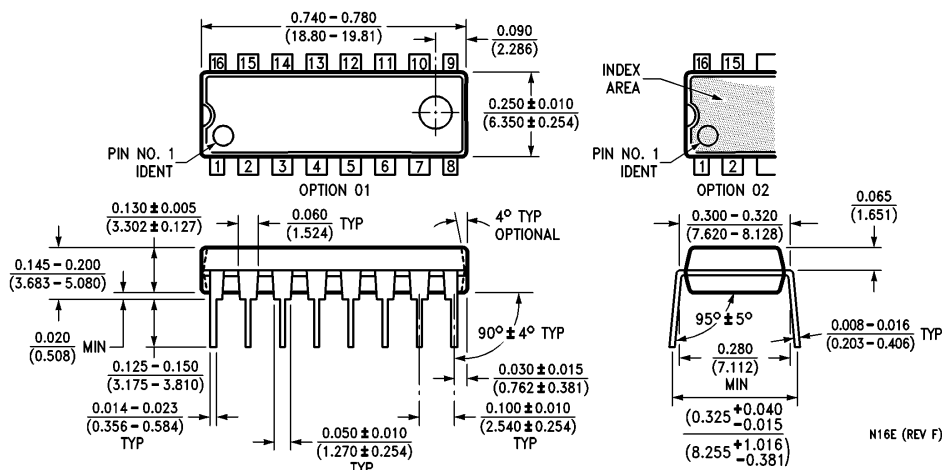
The image contains three mechanical drawings of the J16A (REV L) package:

- Top View:** Shows a rectangular package with 16 pins (8 on each long side). Dimensions include a total width of  $0.785 [19.94] \text{ MAX}$ , a pin pitch of  $0.037 \pm 0.005 [0.94 \pm 0.13] \text{ TYP}$ , and a pin diameter of  $0.025 [0.64]$ . The package body has a width of  $0.220-0.310 [5.59-7.87]$  and a thickness of  $0.005-0.020 \text{ TYP} [0.13-0.51]$ . A corner radius of  $R 0.025 [0.64]$  is specified.
- Side View:** Shows the package height and pin details. The maximum height is  $0.200 [5.08] \text{ MAX TYP}$ . The pin height is  $0.125-0.200 [3.18-5.08] \text{ TYP}$ . The pin diameter is  $0.080 [2.03] \text{ MAX}$  at both ends. The pin angle is  $90^\circ \pm 4^\circ \text{ TYP}$ . The pin spacing is  $0.018 \pm 0.003 [0.46 \pm 0.08] \text{ TYP}$ . The package body thickness is  $0.020-0.060 [0.51-1.52] \text{ TYP}$ .
- Cross-sectional View:** Shows the internal structure with a glass sealant. The package body thickness is  $0.290-0.320 [7.37-8.13]$ . The pin diameter is  $0.180 \text{ MAX} [4.57]$ . The pin angle is  $95^\circ \pm 5^\circ \text{ TYP}$ . The package body width is  $0.310-0.410 [7.87-10.41]$ . The pin diameter is  $0.010 \pm 0.002 [0.25 \pm 0.05] \text{ TYP}$ .

J16A (REV L)

J16A (REV L)

## Physical Dimensions inches (millimeters) (Continued)



### Molded Dual-In-Line Package (N)

Order Number MM70C95N, MM70C96N, MM70C97N, MM70C98N,  
MM80C95N, MM80C96N, MM80C97N or MM80C98N

NS Package Number N16E

N16E (REV F)

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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