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NTE8255
Integrated Circuit
Programmable Peripheral Interface

Description:

The NTE8255 is a general purpose programmable INPUT/OUTPUT device in a 40–Lead DIP type package designed for use with the 8080A/8085A microprocessors. Twenty–four (24) I/O lines may be programmed in two groups of twelve (Group I and Group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bi–directional Bus mode, (MODE 2), uses the 8 lines of Port A for a bi–directional bus, and five lines from Port C for bus control signals.

Features:

- Fully Compatible with the 8080A/8085A Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 4mA Darlington Drive Outputs for Printers and Displays
- LSI Drastically Reduces System Package Count

Absolute Maximum Ratings: (T_A = +25°C, Note 1, unless otherwise specified)

Voltage on Any Pin With Respect to V_{SS} . . . . . –0.5V to +7.0V
Operating Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. With respect to V_{SS}

Note 2. Stress above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics: (T_A = 0° to +70°C, V_{CC} = +5V ±10%, V_{SS} = 0V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		–0.5	–	0.8	V
Input High Voltage	V_{IH}		2	–	V_{CC}	V
Output Low Voltage	V_{OL}	Note 4	–	–	0.45	V
Output High Voltage	V_{OH}	Note 5	2.4	–	–	V
Darlington Drive Current	I_{OH}	V_{EXT} = 1.5V, R_{EXT} = 750Ω, Note 3	–1	–	–4	mA
Power Supply Current	I_{CC}	V_{CC} = +5V, Output Open	–	–	120	mA
Input Leakage Current	I_{LIH}	V_{IN} = V_{CC}	–	–	10	µA
	I_{LIL}	V_{IN} = 0.4V	–	–	–10	µA
Output Leakage Current	I_{LOH}	V_{OUT} = V_{CC} , $\overline{CS}$ = 2V	–	–	±10	µA
	I_{LOL}	V_{OUT} = 0.4V, $\overline{CS}$ = 2C	–	–	–10	µA

Note 3. Any set of eight (8) outputs from either Port A, B, or C can source 4mA into 1.5V.

Note 4. I_{OL} = 2.5mA for DB Port; 1.7mA for Peripheral Ports.

Note 5. I_{OH} = –400µA for dB Port; –200µA for Peripheral Ports.

Capacitance: (T_A = +25°C, V_{CC} = V_{SS} = 0V onless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f_c = 1MHz, Unmeasured pins returned to V_{SS}	–	–	10	pF
I/O Capacitance	$C_{I/O}$		–	–	20	pF

AC Characteristics: (T_A = 0° to +70°C, V_{CC} = +5V ±5%, V_{SS} = 0V unless otherwise specified)

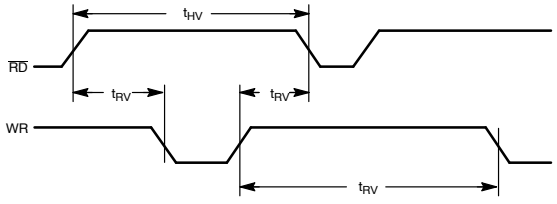
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
READ						
Address Stable Before $\overline{READ}$	t_{AR}		0	–	–	ns
Address Stable After $\overline{READ}$	t_{RA}		0	–	–	ns
$\overline{READ}$ Pulse Width	t_{RR}		200	–	–	ns
Data Valid From $\overline{READ}$	t_{RD}	C_L = 150pF	–	–	140	ns
Data Float After $\overline{READ}$	t_{DF}	C_L = 100pF	–	–	100	ns
		C_L = 15pF	10	–	–	ns
Time Between $\overline{READS}$ and/$\overline{WRITES}$	t_{RV}	Note 7	200	–	–	ns
WRITE						
Address Stable Before $\overline{WRITE}$	t_{AW}		0	–	–	ns
Address Stable After $\overline{WRITE}$	t_{WA}		20	–	–	ns
$\overline{WRITE}$ Pulse Width	t_{WW}		200	–	–	ns
Data Valid to $\overline{WRITE}$ (T.E.)	t_{DW}		100	–	–	ns
Data Valid After $\overline{WRITE}$	t_{WD}		0	–	–	ns

AC Characteristics (Cont'd): (T_A = 0° to +70°C, V_{CC} = +5V ±5%, V_{SS} = 0V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OTHER TIMING						
$\overline{WR}$ = 0 to Output	t_{WB}	C_L = 150pF	–	–	350	ns
Peripheral Data Before $\overline{RD}$	t_{IR}		0	–	–	ns
Peripheral Data After $\overline{RD}$	t_{HR}		0	–	–	ns
$\overline{ACK}$ Pulse Width	t_{AK}		300	–	–	ns
$\overline{STB}$ Pulse Width	t_{ST}		350	–	–	ns
Per. Data Before T.E. of $\overline{STB}$	t_{PS}		0	–	–	ns
Per. Data After T.E. of $\overline{STB}$	t_{PH}		150	–	–	ns
$\overline{ACK}$ = 0 to Output	t_{AD}	C_L = 150pF	–	–	300	ns
$\overline{ACK}$ = 0 to Output Float	t_{KD}	C_L = 50pF	–	–	250	ns
		C_L = 15pF	20	–	–	ns
$\overline{WR}$ = 1 to OBF = 0	t_{WOB}	C_L = 150pF	–	–	300	ns
$\overline{ACK}$ = 0 to OBF = 1	t_{AOB}		–	–	350	ns
$\overline{STB}$ = 0 to IBF = 1	t_{SIB}		–	–	300	ns
$\overline{RD}$ = 1 to IBF = 0	t_{RIB}		–	–	300	ns
$\overline{RD}$ = 0 to INTR = 0	t_{RIT}		–	–	400	ns
$\overline{STB}$ = 1 to INTR = 1	t_{SIT}		–	–	300	ns
$\overline{ACK}$ = 1 to INTR = 1	t_{AIT}		–	–	350	ns
$\overline{WR}$ = 0 to INTR = 0	t_{WIT}	C_L = 150pf, Note 8	–	–	450	ns

Note 6. Period of Reset pulse must be at least 50µs during or after power on. Subsequent Reset pulse can be 500ns Min.

Note 7.



Note 8. INTR↑ may occur as early as $\overline{WR}$↓.

Basic Operation:

Input Operation (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → Data Bus
0	1	0	1	0	PORT B → Data Bus
1	0	0	1	0	PORT C → Data Bus

Note 9. All conditions not listed are illegal and should be avoided.

Note10. X means "DO NOT CARE".

Basic Operation (Cont'd):

Output Operation (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	Data Bus → PORT A
0	1	1	0	0	Data Bus → PORT B
1	0	1	0	0	Data Bus → PORT C
1	1	1	0	0	Data Bus → CONTROL

Disable Function					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	Data Bus → High Z State
X	X	1	1	0	Data Bus → High Z State

Functional Description:

General
The NTE8255 Programmable Peripheral Interface (PPI) is designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the NTE8255. The NTE8255 is functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer
The 3−State, bi−directional, 8−Bit Data Bus Buffer ($D_0 - D_7$) of the NTE8255 can be directly interfaced to the processor's system Data Bus ($D_0 - D_7$). The Data Bus Buffer is controlled by execution in IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic
This block manages all of the internal and external transfers of Data, Control, and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$ (Pin6)
A Logic Low, V_{IL}, on this input enables the NTE8255 for communication with the 8080A/8085A.

Read, $\overline{RD}$ (Pin5)
A Logic Low, V_{IL}, on this input enables the NTE8255 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$ (Pin36)
A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0 (Pin9)
Port Select 1, A_1 (Pin8)
These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset (Pin35)
A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Functional Description (Cont'd):

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the NTE8255. Information such as "MODE", "Bit SET", and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C ($PC_7 - PC_4$)
Group II – Port B and lower Port C ($PC_3 - PC_0$)

While the Control Word Register can be written into, the contents cannot be read back to the processor.

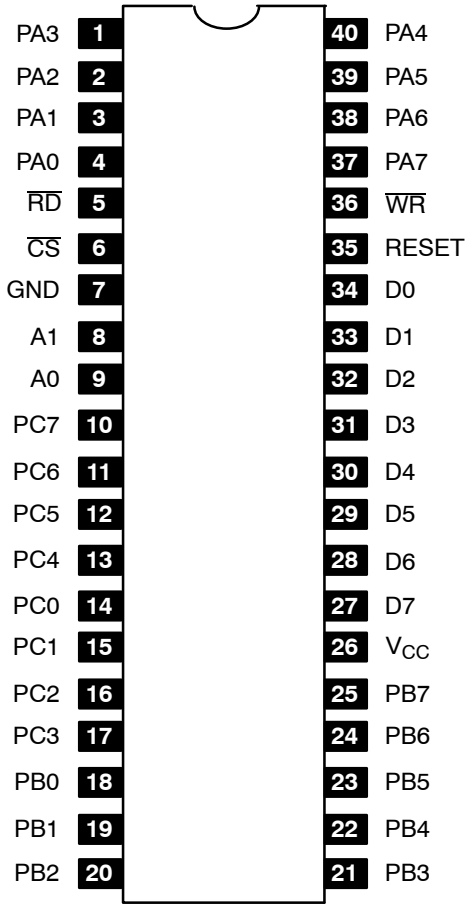
Ports A, B, and C

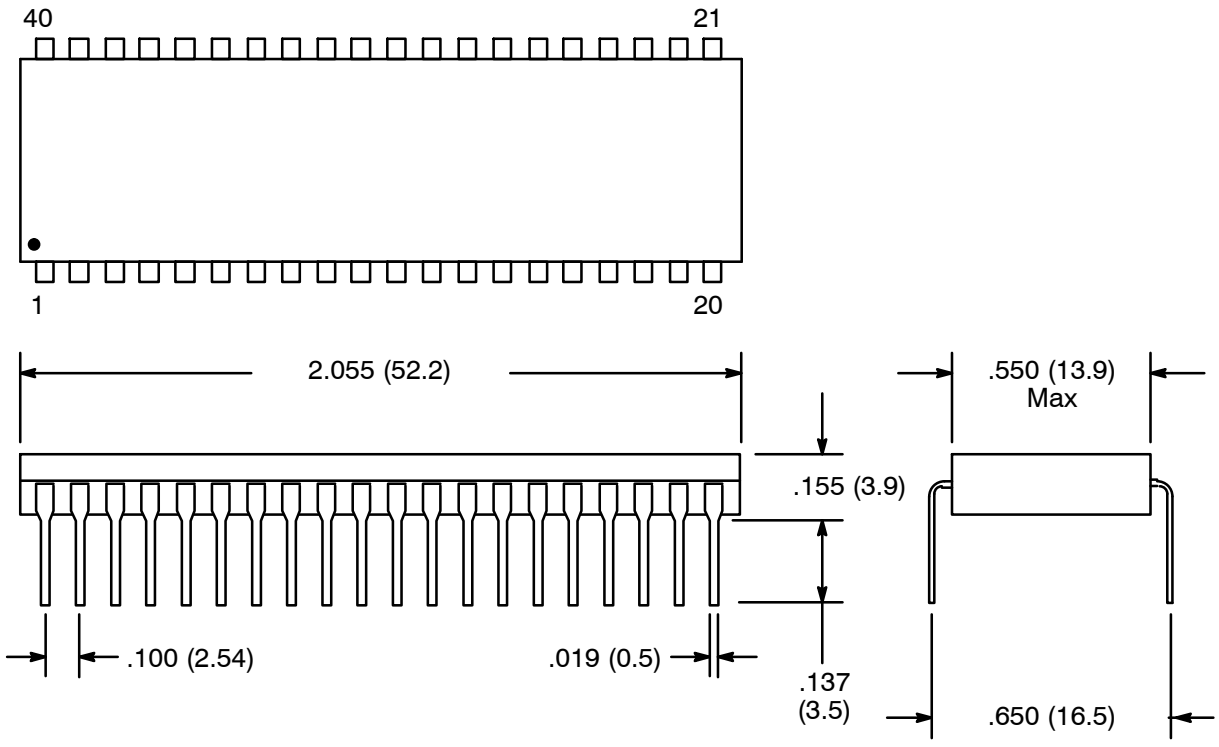
The three 8−bit I/O ports (A, B, and C) in the NTE8255 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the NTE8255 are further enhanced by special features unique to each of the ports.

Port A = An 8−bit data output latch/buffer and data input latch.
Port B = An 8−bit data input/output latch/buffer and an 8−bit data input buffer.
Port C = An 8−bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4−bit control and status ports for use with Ports A and B.

Pin Connection Diagram




40
21
1
20
2.055 (52.2)
.550 (13.9)
Max
.155 (3.9)
.100 (2.54)
.019 (0.5)
.137
(3.5)
.650 (16.5)